



# User Guide

## EVB-ATEK150P3-01

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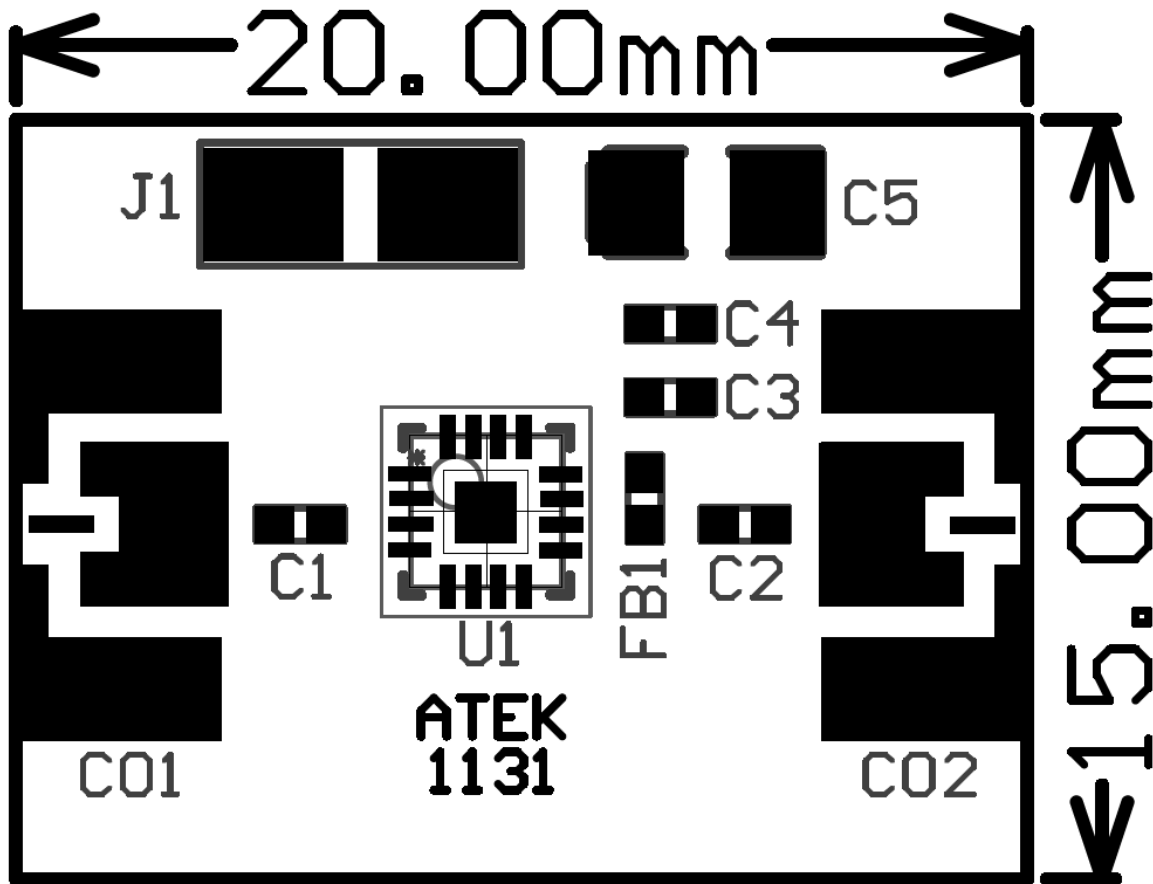
**Revisions**

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	28.07.2021	Initial Release	
1.1	08.01.2022	Format and Content Fixed	
1.2	18.02.2022	Content Fixed	
1.3	16.04.2022	Content Fixed	

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1 GENERAL INFORMATION



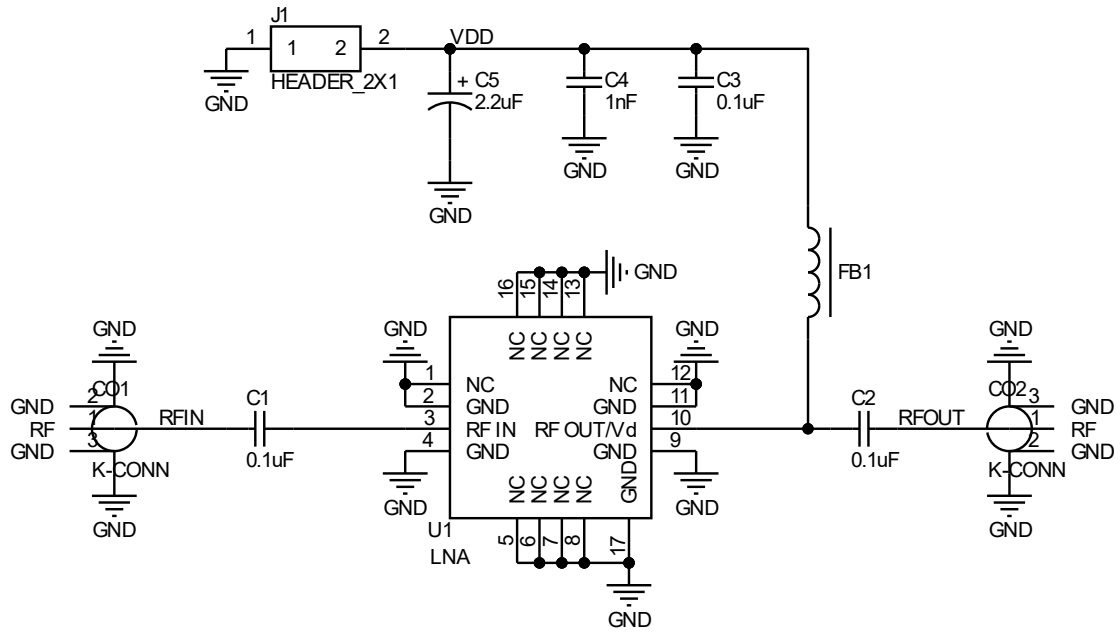
PIN Name	Definition	Comment
<b>CO1</b>	RF IN	SMA Connector
<b>CO2</b>	RF OUT	SMA Connector
<b>J1 Right</b>	VDD	2.54mm Header
<b>J1 Left</b>	GND	2.54mm Header

Notes:

1. VDD Voltage is detailed in Datasheet.
2. The definition of right and left is valid for this view of PCB.

2 DESIGN INFORMATION

2.1 SCHEMATIC



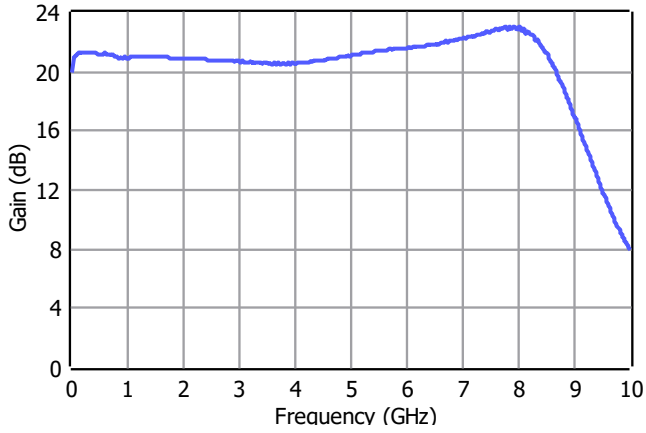
2.2 BOM

Designator	Footprint	Qty	Comment	PN
<b>C1, C2</b>	0402	2	100nF	
<b>C3</b>	0402	1	100pF	
<b>C4</b>	0402	1	10nF	
<b>C5</b>	CASEA	1	2.2uF	
<b>CO1, CO2</b>	SMA Connector	2	SMA Connector	
<b>FB1</b>	0402	1	Ferrite Bead	
<b>J1</b>	2x1 Header	1	2x1 Header	
<b>U1</b>	ATEKQ3316	1	LNA	ATEK150P3

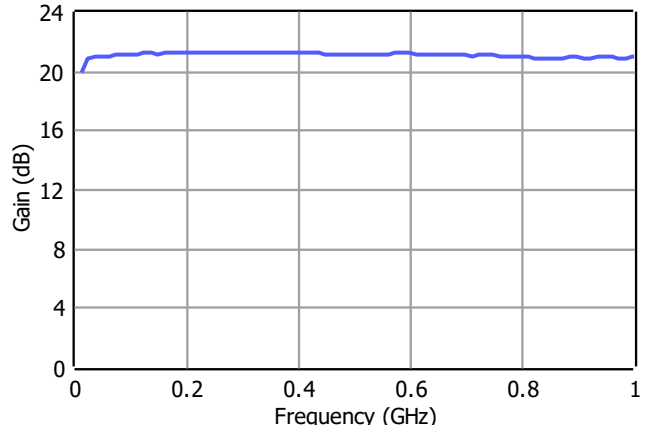
3 TYPICAL PERFORMANCE PLOTS

Conditions unless otherwise specified: VDD = 5 V, T=25 C, CW. For details, please refer to the datasheet.

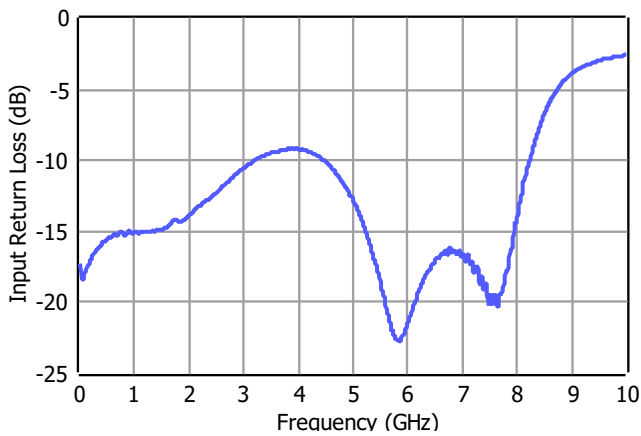
Gain Wideband



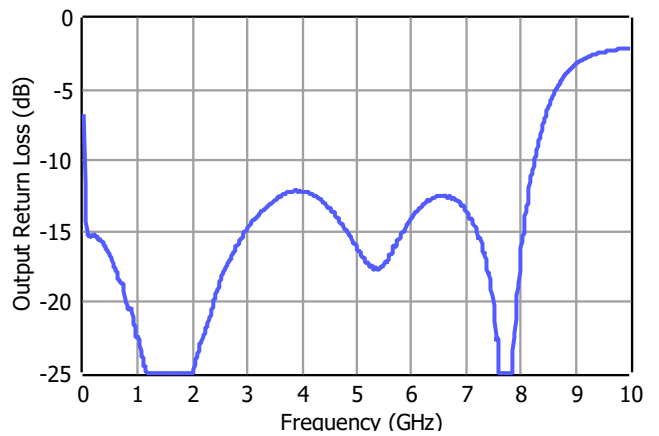
Gain Low Frequency



Input Return Loss



Output Return Loss



Isolation

