Product Description

ATEK153 is a low noise amplifier fabricated on GaN process. Amplifier operation range covers 6 - 13 GHz.

Due its process inherent features, amplifier can survive large RF input signal levels, which eliminates the need of lossy limiter circuitry usage at the amplifier input. This results in improved receiver noise figure and increased total system dynamic range.

Amplifier has two Vgg pads, which allows user to choose the class of operation, dynamically depending on the scenario of operation. Under large RF input drive, amplifier can be biased for improved linearity to increase the overall system dynamic range. If the RF input signal is low, the amplifier can be biased for low power consumption to save power.

Evaluation Board, bare die, custom package, and module options are available upon request.

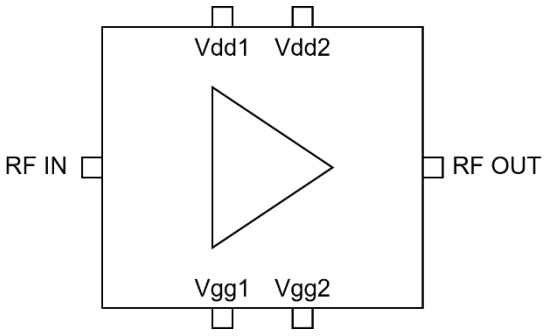
Product Features

- Frequency Range: 6 - 13 GHz
- Gain: 13 dB
- Noise Figure: 2.2 dB
- P1dB: 27.5 dBm
- Psat: 30 dBm
- 1.15 x 2 mm compact chip size

Applications

- Radar
- Electronic Warfare
- Test Equipment

Functional Block Diagram



Electrical Specifications

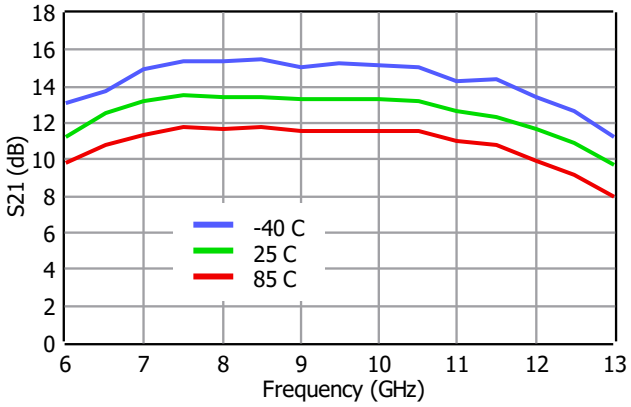
Conditions unless otherwise specified: V_{DD} = 10 V, I_{DQ} = 167 mA, Typical, CW.

Parameter		Min	Typ	Max	Units
Operational Frequency Range		6		13	GHz
Gain	6 GHz		11.7		dB
	8 GHz		13.5		
	10 GHz		13		
	12 GHz		12		
	13 GHz		10		
Noise Figure (Vdd = 15 V, Idq=140 mA)	8 GHz		2.4		dB
	10 GHz		2		
	12 GHz		2.2		
	13 GHz		2.5		
Input Return Loss			-9		dB
Output Return Loss			-12		dB
Output P1dB (Vdd = 15 V, Idq = 306 mA)			29		dBm
Psat (Vdd = 15 V, Idq = 306 mA)			31		dBm
DC Supply Voltage (Vdd1, Vdd2)		5		20	V
Operating Temperature		-40		85	°C

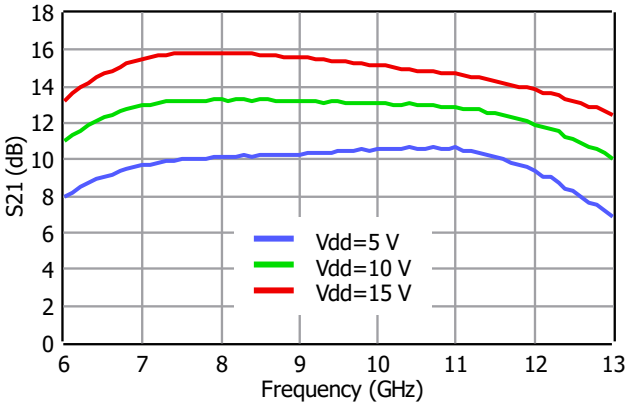
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 10 V, I_{DQ} = 167 mA, Typical, CW.

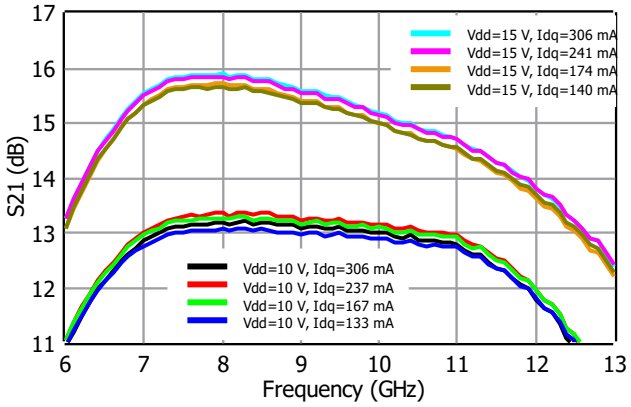
Gain vs. Temperature



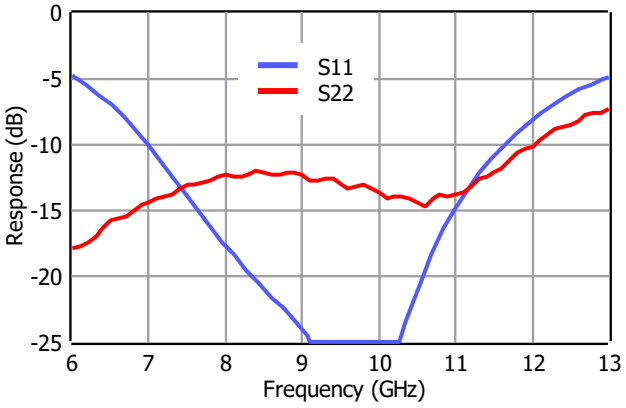
Gain vs. Vdd



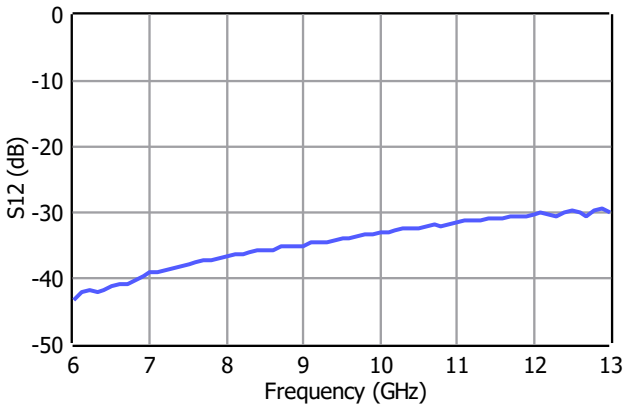
Gain vs. Vdd, Idq



Return Losses



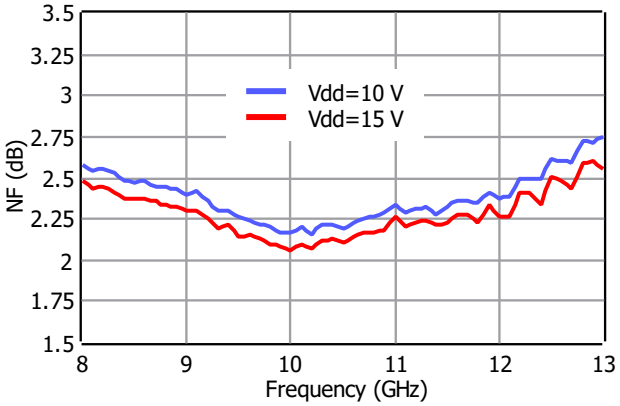
Isolation



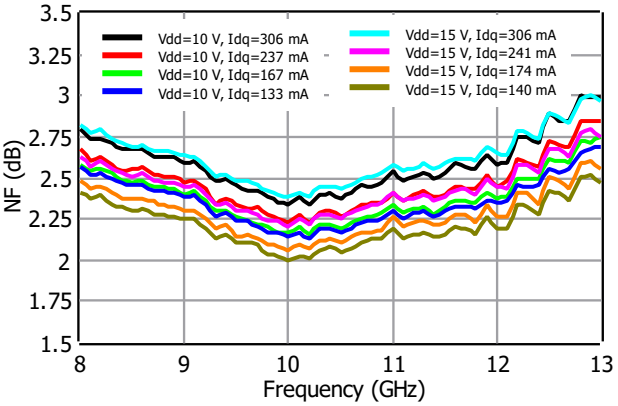
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 10 V, I_{DQ} = 167 mA, Typical, CW.

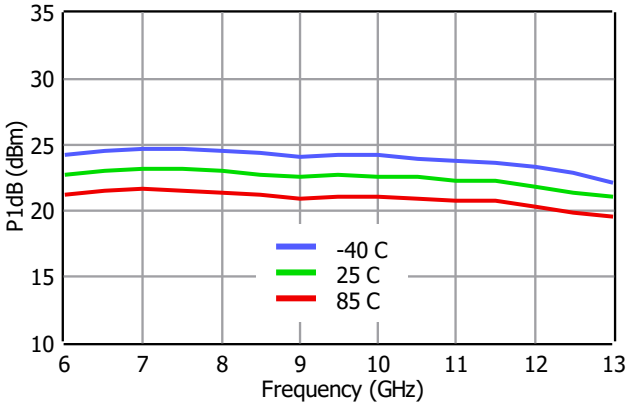
Noise Figure vs. Vdd



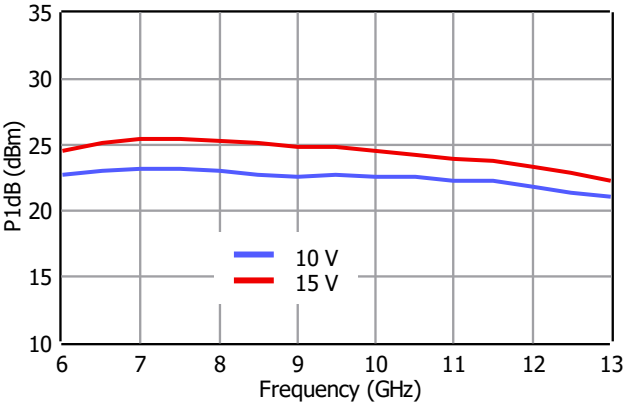
Noise Figure vs. Vdd, Idq



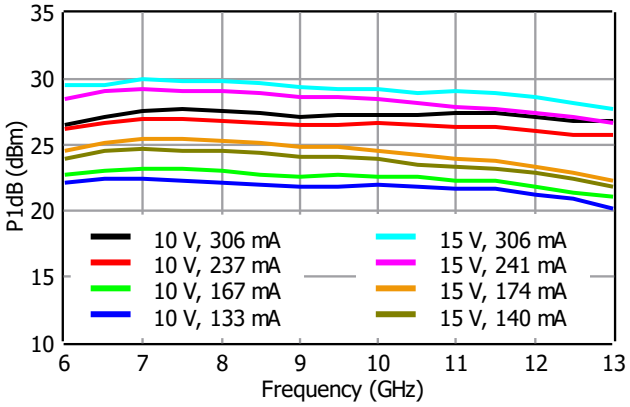
P1dB vs. Temperature



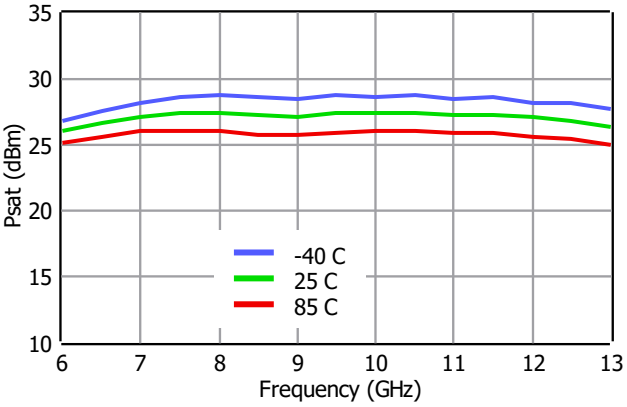
P1dB vs. Vdd



P1dB vs. Vdd, Idq



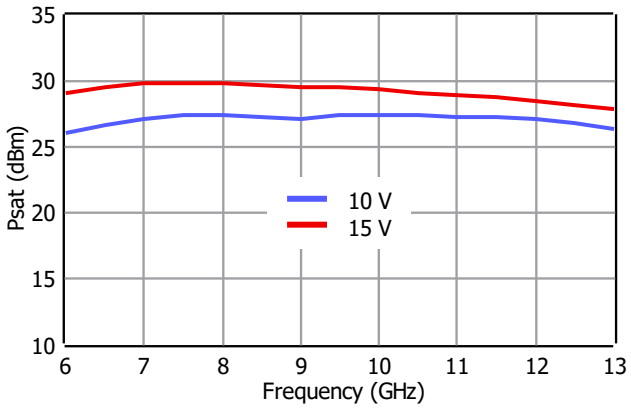
Psat vs. Temperature



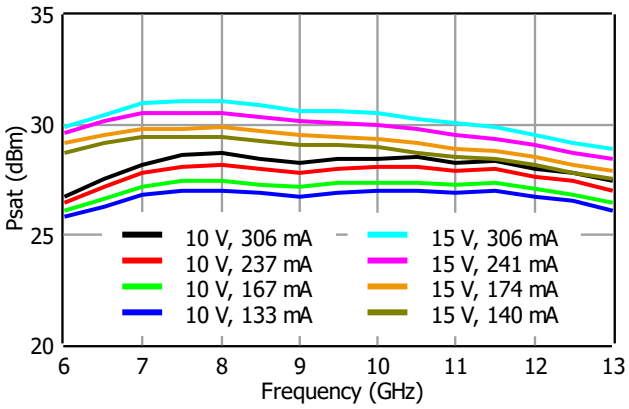
Typical Performance Plots

Conditions unless otherwise specified: V_{DD} = 10 V, I_{DQ} = 167 mA, Typical, CW.

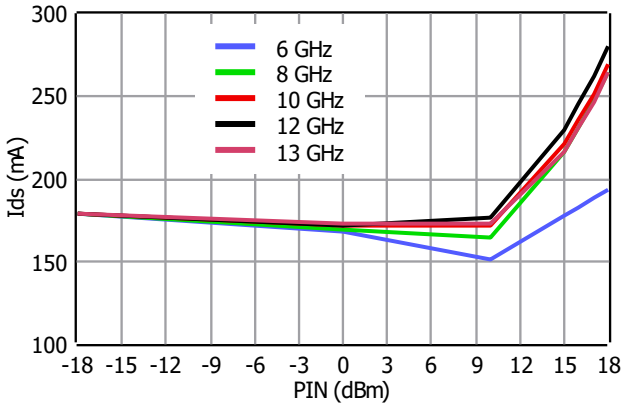
Psat vs. Vdd



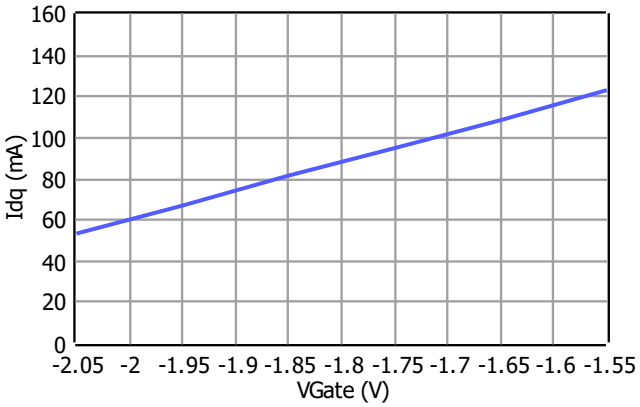
Psat vs. Vdd, Idq



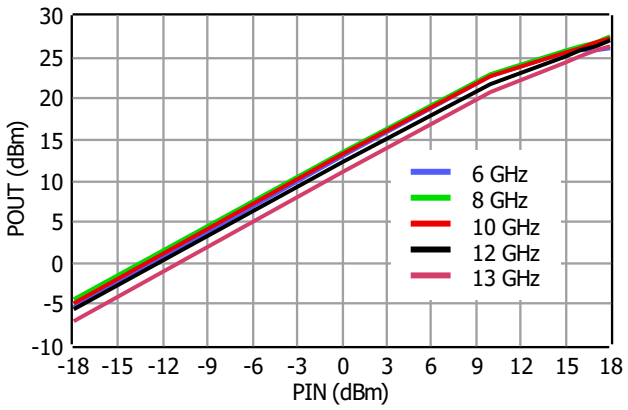
Ids vs. Pin, Frequency



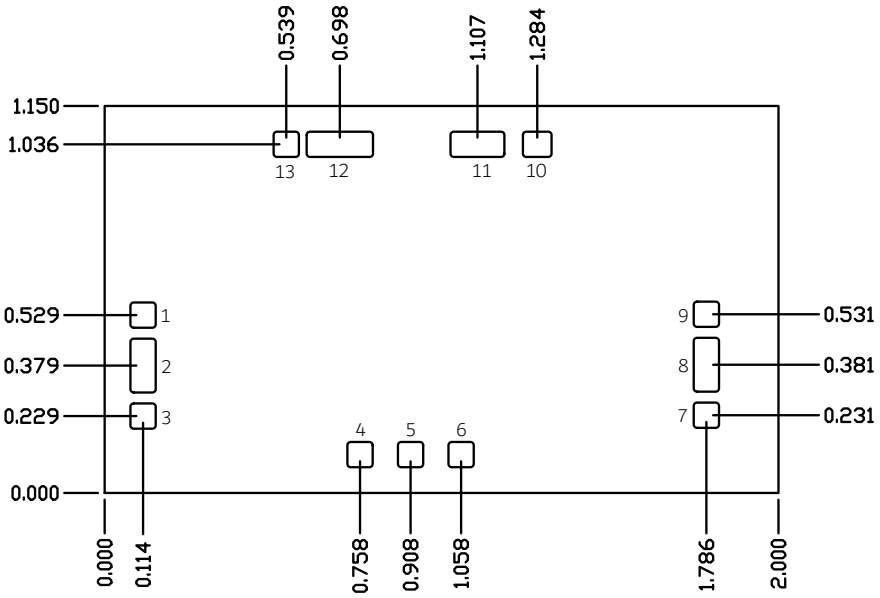
Idq vs. Vgg



Pout vs. Pin, Frequency



Pad Description and Mechanical Dimensions

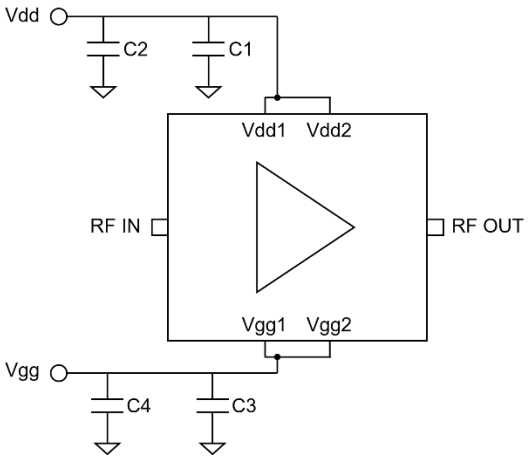


Units: millimeters
Thickness: 0.10
Die x, y size tolerance: ±0.05
Backside of die is ground

Pad Number	Pad Name	Description
2	RF IN	RF input/output pin. If the DC voltage level on RF lines is not equal to 0 V, an external DC block capacitor is required.
8	RF OUT	RF input/output pin. If the DC voltage level on RF lines is not equal to 0 V, an external DC block capacitor is required.
12	VDD1	Drain Bias Pin.
11	VDD2	Drain Bias Pin.
4	VGG1	Gate Bias Pin.
5	VGG2	Gate Bias Pin.
1, 3, 6, 7, 9, 10, 13	GND	Ground.
-	Backside	Backside of the die should be connected to ground with appropriate solder or epoxy with high electrical and thermal conductivity.

Applications Information

Signal entering from RF1 goes to RF2 with an amplification with low noise figure.
Typical application schematic to operate the low noise amplifier is given below.



The amplifier has internal DC block capacitors which eliminated the need to use external DC block capacitors.
C1, C2, C3 and C4 are used to filter out the ripples and unwanted signals coming from the Vdd and Vgg supplies. Using additional capacitors in parallel to C1, C2, C3 and C4 will improve this filtering. If this filtering is of no concern, then amplifier can be operated without C1, C2, C3 and C4.
Vgg1 and Vgg2 pins can be operated separately to bias input and output stages of the amplifier in different configurations. For instance, input stage can be operated for lower noise and the output stage can be configured for higher linearity. All plots in this document are generated when Vgg1 and Vgg2 pins are shorted together. If Vgg1 and Vgg2 biases are to be controlled separately, user needs to characterize the amplifier accordingly.

Absolute Maximum Ratings

Parameter	Value/Range
Supply Voltages (Vdd1, Vdd2)	TBD
Gate Bias Voltages (Vgg1, Vgg2)	TBD
RF Input Power	TBD
Storage Temperature	−55 to +125°C

Operation of this device outside the parameter ranges given above may cause damage. These parameters should not be applied simultaneously.

Handling Precautions

Caution!
ESD-Sensitive Device
Handle Accordingly

Contact Information

For the latest specifications, additional product information, support, and sales.
Web: www.atekmidas.com
Tel: +90-212-483-71-67
Email: support@atekmidas.com

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Revisions

Revision No	Revision Date	Revision Reason	Section / Page No
1.0	2021	Initial Release	
1.1	30.03.2022	Content Fixed	